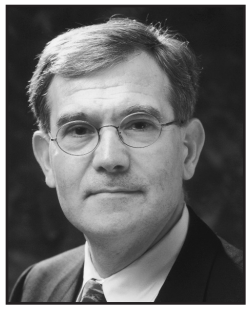
# Foreword

## The 4 Dimensions of IC Innovation



It is my pleasure to welcome you to the 54th International Solid-State Circuits Conference. The Conference continues its outstanding tradition of presenting the most-advanced and innovative work, both in industry and academe, worldwide, in the area of integrated circuits and systems. For the first time in the history of ISSCC, the number of papers accepted from academe (51%) exceeds that from industry (49%). We also notice an increasing contribution from the Far East (31% of accepted papers) and Europe (30%), an interesting indicator of some global trends in the way research and development is being done.

This year's Conference theme is "**The 4 Dimensions of IC Innovation**," in recognition of the emerging synergisms between the various aspects of integrated circuits. The continued extension of Moore's Law has pushed integrated circuits - their creation, their fabrication, and their application - from the microelectronic into the nanoelectronic era. This transition has created tremendous opportunities for higher-density higher-performance and lower-power circuits and systems, creating cost-effective solutions for ubiquitous communications, computation, sensing, display, consumer electronics, and multimedia. However, the advent of the nano-era has blurred the traditional boundaries between the four dimensions of IC innovation: technology, devices, circuits, and system architectures. In fact, innovation in solid-state circuits has become a delicate optimization between advances in process, circuit, architecture, and system technologies. The Plenary speakers will shine more light on these aspects.

One of the highlights of ISSCC is the Plenary Session, where leaders and authorities in the field share their insight and experience with the audience. This year, we have three outstanding speakers whose presentations cover various facets of the complex world of IC innovation. The first speaker is Morris Chang, founder of TSMC, who will talk about the future and challenges of silicon foundries, and how foundries will continue to be a driving force for the semiconductor industry, by providing advanced technologies in an ever- increasingly-competitive environment. The second Plenary presentation, by Lewis Counts of Analog Devices, focuses on analog and mixed-mode circuit innovation in the nanoscale regime. The third talk by Joël Hartmann, of Crolles2 Alliance, explains how increased parameter variability in today's nanoscale technologies requires a global optimization among the four dimensions of process-technology, device, circuit, and system design, leading to a Generalized Design-for-Manufacturability (GDfM).

The ISSCC Technical Program consists of 234 outstanding papers, distributed over 31 thematic sessions. In the Analog area, we notice an increased emphasis on power-management techniques, power-supply scaling, and low-phase-noise circuits (Sessions 17, 29). Data Converters have made a shift to 90nm technology, with 1V supply voltage (Sessions 13 and 25). The delta-sigma ADCs described cover wider bandwidths and provide multimode operation for use in multiple radio standards (Session 13). The focus of several Nyquist converters is on power and area efficiency (Session 25). Circuit topologies that are able to operate with supply voltages of 1 to 1.2V are being explored. In the Digital arena, microprocessors fabricated in 65nm technology exhibit a rapid rate of performance improvement (Session 5). This year. we see a new record for microprocessor clocking, with 5GHz operating frequency. An 80-tile network-on-chip (NoC) microprocessor achieves 1.28 TFlops with a 4GHz clock. Also, an 8-core power-efficient SPARC will be presented, that is able to handle up to 64 programs simultaneously. Besides record levels of performance, the microprocessor papers exhibit independent core-level frequency control and power management. Novel clock-distribution schemes are being explored, such as using magnetic links for the clock mesh and standing-wave clock distribution, and an all-digital low-voltage, area-efficient PLL with low-jitter to enable higher clock frequencies at lower power dissipation (Session 9). Processor performance is further optimized through adaptive techniques using active damping circuits, multiple on-chip sensors (Session 16), and distributed monitor circuits that correct for transistor variations and power-supply droops (Session 22). The Display area presents mobile displays with increased color depth and integration levels, to increase functionality and decrease power and cost (Session 7). Session 8 showcases the latest advances in multi-channel retinal prosthesis and implantable brain-wave-recording probes, with up to 256-channels. opening the door for high-resolution retinal prosthesis, and high-throughput drug screening. The MEMS session (Session 21) introduces a single-chip electronic compass with a 3-axis magnetic sensor providing a short-time heading precision better than 0.5°, enabling hand-held applications. A low-power micro-gyroscope MEMS with a record-high accuracy of 0.2° per hour will be presented in Session 21. Imagers witness continued shrinking of the pixel size (down to 1.75µm), and increased resolution. High-performance lower-cost cameras with 8.1Mpixels CMOS sensors in the 1/ 2.5-inch format (Session 28) are replacing 5Mpixels sensors. We also notice that 1/ 2.7-inch low-noise CMOS imagers are approaching CCD quality for HD camcorder applications. In the Memory area, SRAMs are moving into the sub-threshold regime, operating down to 330mV and the sub-200mV retention regime. Novel techniques to reduce the leakage current allow for mobile applications (Session 18). Phase-change memory sets new records in terms of density and performance, as does the 1Gbit multi-level NOR-Flash with the fastest write and read throughputs ever reported (Session 26). The DRAM session will feature the first high-performance 65nm embedded DRAM in SOI, and the first GDDR4 Graphics DRAM with bandwidth over 4Gb/s/pin (Session 27). High-efficiency RF circuits and improved concepts enable low-cost feature-rich mobile phones (Session 4). Session 10 will present the first receiver circuits operating at 60 GHz realized in digital CMOS, as well as the first CMOS VCO operating at 100GHz. Novel beamforming techniques incorporated on a highly integrated silicon-based radar IC will enable low-cost applications for automotive-collision avoidance radars, and high-frequency radio-wave imaging for medical and security applications (Session 23). In the area of Signal Processing, Session 14 will demonstrate an SoC for next-generation cell-phone applications, that includes audio, RF, digital, memory, and power-management. This is a major step toward achieving a single-chip low-cost GSM phone. The first fully-integrated 3x3 MIMO-baseband processor, utilizing multiple datastreams, exhibits an exceptionally-high throughput of 300Mb/s, and unprecedented wide range, showcasing the future of WLAN for multimedia data streaming. A real-time 3D display processor, in combination with a 3D-graphics- rendering engine synthesizes SXGA images at a frame rate of 36f/s (Session 15). The Technology Directions sessions continue to show us a glimpse of the next-generation post-CMOS technologies and systems. Energy-efficiency is a common theme among the papers in Session 7. Circuits and energy-scavenging techniques for battery-less systems for ultra-low-power devices will be presented. Carbon-nanotube circuits are approaching the performance of ultra-scaled CMOS circuits. Papers in Session 20 show how capacitive and inductive chip-to-chip interconnect can be used for ultra-low power communication. Architectures for adaptive software-defined radios which achieve up to 40% lower energy will be described in Session 32. As well, in Session 32, compact high-resolution millimeter and sub-millimeter wave cameras with amplifiers operating at 300Gz for see-through imaging applications will be described. In the Wireless arena, the first complete integrated 65nm CMOS WiMedia-compliant UWB transceiver and all-digital 90nm CMOS ultra-low-power dual-band pulsed-based transmitter for high data rates (800Mb/s) will be described (Session 6), leading the way to cost-effective UWB realizations. A single-chip integration of a UHF RFID-reader transceiver with high data rates and extended range is described in Session 11. Also the first direct-conversion TV turner that covers the full 48-to-860MHz bandwidth, without harmonic-mixing problems, will be described in Session 11. Several novel WCDMA transmitter topologies that achieve the spectral-emission limits without an external SAW filter are the topic of Session 19, enabling lower-cost 3G cellular phones. The Wireline area highlights a fully-integrated 4x10Gb/s DWDM optoelectronic transceiver that makes use of a silicon interleaver with 4-channel Mach-Zender-interferometer drivers, and receivers on a single 0.13µm CMOS SOI chip. Also, a novel clocking solution is described for sub-picosecond jitter performance using a low-cost crystal suitable for 10Gb/s SONET applications (Session 2). Session 12 highlights 40Gb/s CDRs and equalizers which

achieve record-breaking to low power consumption. Multi-Gb/s transceivers using all-digital approaches in a sub-90nm CMOS technology enables inexpensive, low-power high-speed communications (Session 24). A 100GHz CMOS clock divider, as part of a transceiver, breaks another speed barrier. The divider is fabricated in a 65nm SOI technology, and consumers only 52.4mW.

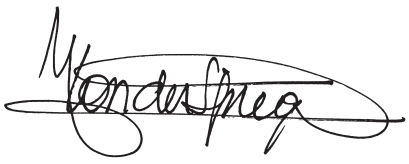
Besides the Regular Paper presentations, the Conference continues to offer a wide variety of high-quality educational programs, adding to the already significant value of attending ISSCC. This year, there are ten Tutorials dealing with current issues in analog, digital, and RF circuits, wireless and wireline communication systems, signal processing, power management, data converters, sensor-interface circuits, and organic-transistor circuits. These Tutorials are given by top experts in the field, and offer an opportunity to the participants to near an introduction and overview of important developments in each of these areas. The Conference is also offering seven Forums whose intent is to cover more-advanced topics for experts in the field. This year, Forums deal with power amplifiers, non-volatile memory, 3-D electronics, adaptive techniques for dynamic processor optimization, low-voltage analog design for filters and ADCs, automotive bus systems, and noise in imaging systems. The Short Course deals with the popular topic of *analog, mixed-signal and RF circuit design in nanometer CMOS*. As well, there are also two types of evening sessions, Panel Discussions and Special-Topic Sessions, which provide a participant with the opportunity to learn about a timely topic in a more- relaxed setting. One of the two Panel Discussions will look at the *ultimate limits of IC fabrication,* and another will discuss the emerging area of *digital RF*. Both Panels will provide for a stimulating evening of discussion and interaction with some of the most-knowledgeable visionaries in the field. Seven Special-Topic Sessions offer plenty of choice to the participants to get informed about a topic of increased importance in the field of solid-state circuits. These topics are carefully selected by the Program Committee for their timeliness and relevance.

The quality and high standards that we associate with ISSCC is by-and-large due to the diligent work of the Technical Program Committee. This year, we have 181 members of the International Technical Program Committee, divided over ten Technical Subcommittees. Of the 181 members, 80 are from North America, 58 from the Far East, and 43 from Europe. Each member has made tremendous contributions by reading and reviewing large numbers of submitted papers, planning and organizing evening sessions and educational activities, preparing the Advance Program, Press-Kit and Digest material in a timely manner. All of them attended two Program Committee meetings, one in June and another in October of 2006. I would, in particular, like to acknowledge the leadership and guidance of the Technical Subcommittee Chairs: Bill Redman-White (Analog), David Robertson (Data Converters), Samuel Naffziger (Digital), Daniel McGrath (Imagers, MEMS, Medical and Displays), Katsuyuki Sato (Memory), John Long (RF), Wanda Gass (Signal Processing), Anantha Chandrakasan (Technology Directions), Trudy Stetzler (Wireless), and Franz Dielacher (Wireline). Also, I would like to thank the members of the Regional Committees: Jinyong Chung, Takayuki Kawahara and Sung Bae Park from the Far-East Region, and Rudolf Koch, Qiuting Huang and Bram Nauta, from the European Region. Their help and support was essential for the smooth preparation of the Conference.

Many other people play an essential role in making the Conference possible. I would like to thank Yoshi Hagihara for his help as the Program Vice-Chair, Shahriar Mirabbasi as the Program Secretary, Diane Melton as Director of Operations, Molly Bartkowski and Amy Roth of Courtesy Associates for their invaluable help with Conference operations and arrangements. Thanks also to Bill Romer for his assistance with the electronic manuscript submission, formatting and prevoting; to Steve Bonney for his expertise and help with the Advance Program, Press Kit, and Digest; to the Technical Editors, Mandana Amiri, Glenn Gulak, Shahriar Mirabbasi, Kostas Pagiamtzis, and Richard Spencer, for their excellent work on the Advance Program and the Digest. Also, special thanks to Laura Fujino and Kenneth Smith for their unrelenting help with many aspects of the Conference including the paper submission process, the Advance Program, the Press Kit, the Digest, the Digest CD, the Visuals Supplement, the 2007 Short-Course CD, the 2007 Tutorial DVD, and the Digest/Visuals-Supplement DVD. Also, thanks to Willy Sansen for coordinating the Tutorials, and Circuit Forums; to Ian Galton for organizing the Short Course; to Frank Hewlett for his help with the Conference Processes and meeting minutes; to John Trnka for his excellent work with planning and coordinating the audio-visual services of the Conference; and to David Pricer for dealing efficiently with Corporate Relations, and providing wise advice on Conference operations.

One of the people who deserves special recognition is Tim Tredwell, chair of the Executive Committee, for the enthusiastic support he has given me, and his visionary leadership that has maintained ISSCC as the Premier Conference in Solid-State Circuits.

Have an enjoyable ISSCC 2007!



Jan Van der Spiegel, ISSCC 2007 Technical Program Chair